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5. ELECTRONICS (IC 555& COUNTERS)

Advantages of ICs - pin configurations of 555 IC - Design of Astable and mono-stable multivibrator using 555 IC - Design of counters using FF-UP/DOWN counters– -Ring counters - Multiplexes –De-multiplexes

Part –A (2 Marks)

1. What do you mean by Mono-stable multi-vibrator (NOV/2014)
   A mono-stable multi-vibrator is a regenerative comparator having one stable state & one quasi stable state.
2. List the applications of 555 timer in Mono-stable mode of operation (NOV/2014)
   - Frequency doubler
   - Pulse width modulation
   - Linear ramp generator
   - Missing pulse detector.
3. What is a multi-vibrator? (APRIL/2014)
   A circuit which can oscillate at a number of frequencies is called a multivibrator.
4. Write the applications of BCD counters. (APRIL/2014)
   - Sequential generator
   - To enable interrupt in Control application
   - Used as timer
5. List the applications of counter.(NOV/2013)
   - Sequencer
   - Frequency divider,
6. List the advantage of ICs. (APRIL/2013)
   - Extremely small size
   - Very less weight
   - Reduced cost
   - High reliability
   - Low power consumption
   - Easy replacement
   - Increased response time and speed

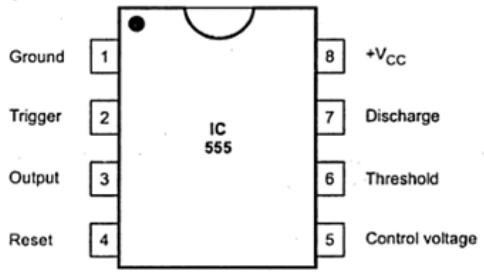
- Higher yield

7. Define shift register. (APRIL/2013)

   The binary information (data) in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses. This type of movement or shifting is essential for certain arithmetic and logical operations used in microprocessors. This gives rise to a group of registers called shift registers.

8. Mention some applications of digital counters. (NOV/2012)
   - Alarm clock
   - Flashing indicator lights of your vehicle
   - Camera

9. Draw the pin configurations of 555 IC. (APRIL/2012) (NOV/2013)



10. What are the types of shift registers? (APRIL/2012)
    - Serial In serial out shift register
    - Serial in parallel out shift register
    - Parallel in serial out shift register
    - Parallel in parallel out shift register
    - Bidirectional shift register

Part- B (11 Marks)

INTEGRATED CIRCUIT(IC)

"An IC is an Electronic circuit in which the active and passive components are fabricated on a tiny single chip of silicon"

Advantages OF ICs

1. *Extremely small size*
   - This is thousands of times smaller than a discrete circuit.
2. *Very less weight*
   - Many circuit functions can be packed into a small space.
3. *Reduced cost*
   - The reduction in cost is due to that many identical circuits can be built simultaneously on a single wafer this process is called Batch fabrication.
4. *High reliability*
   - It is due to the absence of soldered connections
   - Higher reliability means that the ICs will work for longer period without any problem.
5. *Low power consumption*
   - Because of their small size, ICs are more suitable for low power operation.
6. *Easy replacement*
   - ICs are hardly ever repaired because in case of failures, it is more economical to replace them than to repair them.
7. *Increased response time and speed*

- Various components of an IC are located close to each other, therefore the time delay of signals is reduced.
- Because of the short distances, the chance of stray electrical pickup (called parasitic capacitance) is nil. As a result, the response time or the operating speed of the system is improved

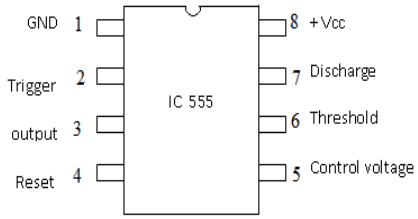
8. *Higher yield*
   - The yield is the percentage of usable devices. Due to batch fabrication, the yield is very high.

Disadvantages of IC

- It functions at fairly low voltages.
- Coils or inductors cannot be fabricated.
- Handle only limited amount of power.
- Cannot withstand rough handling or excessive heat.

1. Draw and explain the functional diagram of a 555 timer. (NOV/2012) (NOV/2014)

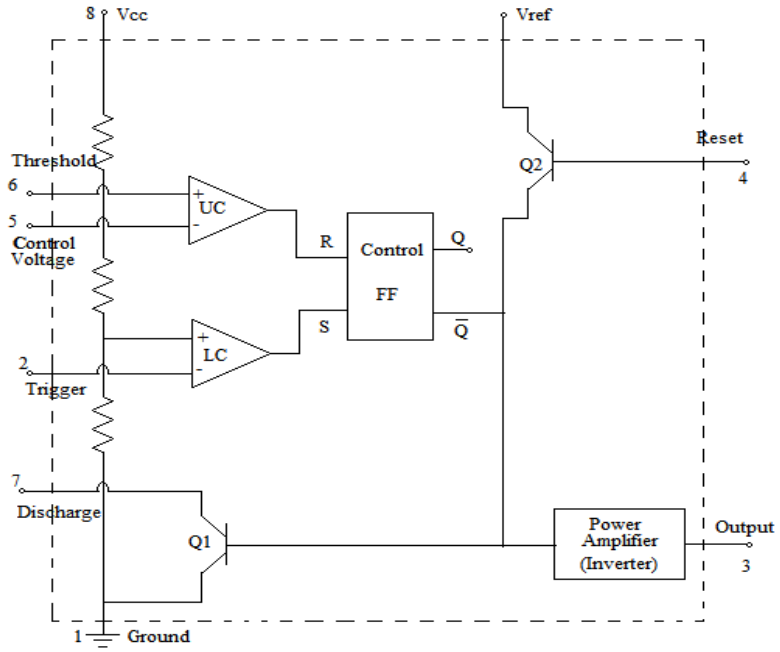
PIN CONFIGURATIONS OF IC 555



Pin diagram of IC555

Pin Functions

- **Pin: 1**: Ground (GND): All voltages are measured with respect to this terminal.
- **Pin:** 2: Trigger: It is the external input that will be applied to the inverting input of the lower comparator & will be compared with (1/3) V_{cc} coming from the potential divider network.
- **Pin:** 3: Output: Complement of the output of the flip-flop acts as the final output of timer as it passes through a power amplifier which is an inverter. Load can either be connected between pin 3 & ground or pin 3 & V_{cc}.
- **Pin**: 4: Reset: This is an input to the timing device which provides a mechanism to reset the flip-flop in a manner which overrides the effect of any instruction coming to the FF from lower comparator. This is effective when the reset input is less than 0.4V.When not used it is returned to V_{cc}.
- **Pin**: 5: Control Voltage input: Generally the fixed voltages of (1/3)V_{cc}&(2/3)V_{cc} also aid in determining the timing interval. The control voltage at 5 can be used when it is required to vary the time & also in such cases when the reference level at V- of the UC is other than 2/3Vcc.Generally when not used a capacitor of 0.01uF should be connected between 5 & ground to bypass noise or ripple from the supply.
- **Pin**: 6: Threshold: An external voltage by means of a timing capacitor & resistor is applied to this pin. When this voltage is greater than (2/)3V_{cc} output of UC is 1 which is given to the set input of FF thereby setting the FF making Q=1 & Q=0.
- **Pin**:7: Discharge: This pin is connected to the collector of the discharge transistor Q_1.When Q output of the FF is 1,then Transistor Q_1 is on due to sufficient base drive hence driving transistor into saturation. When output of the FF is low Transistor Q_1 is off hence acting as a open circuit to any external device connected to it.
- Pin: 8: +Vcc (Power Supply): It can work with any supply voltage between 5 & 18V.



Detailed Diagram of IC555

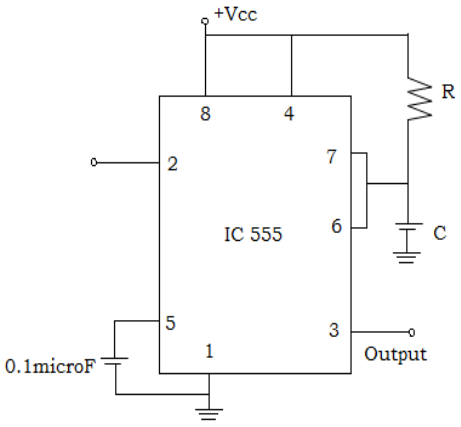
The two major applications of 555 timer are:

- Monostable multi-vibrator.
- Astable multi-vibrator.

2. Explain the operation of monostable multi-vibrator. (APRIL/2013)

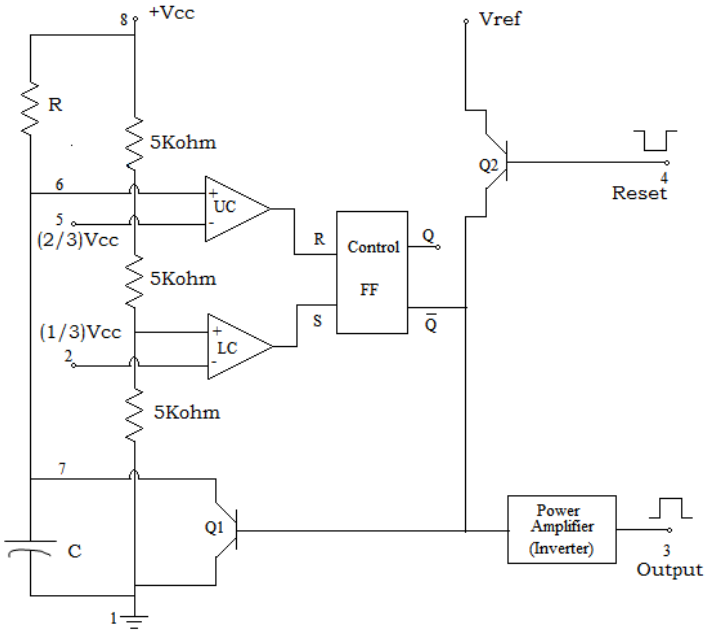
MONOSTABLE MULTIVIBRATOR

A monostable multi-vibrator is a regenerative comparator having one stable state & one quasi stable state. The IC555 timer can be operated as a monostable Multi Vibrator by connecting an external resistor & a capacitor as shown in figure below:



Pin Diagram of Monostable Multi-vibrator

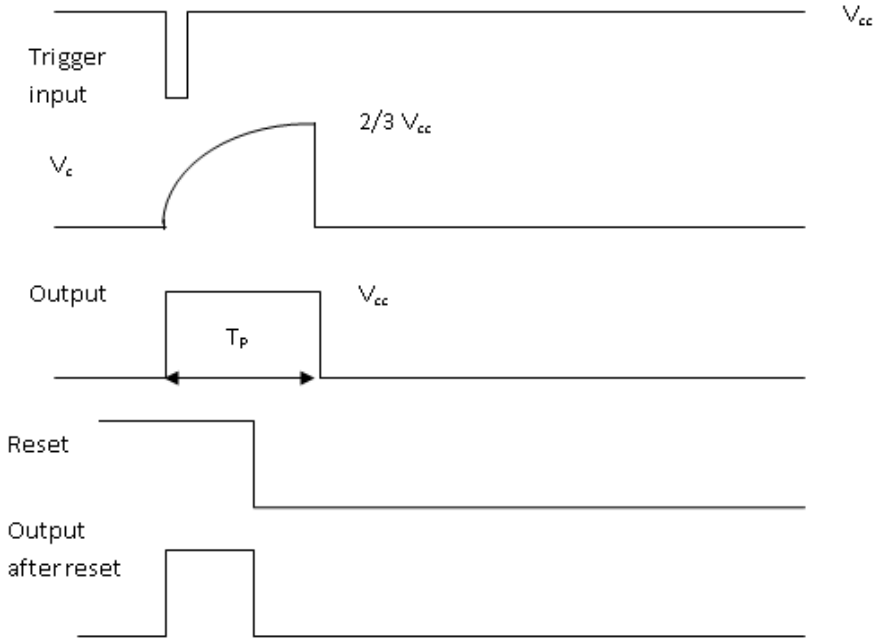
This circuit has only one stable state (0 state) .Whenever an external trigger is applied, it produces a pulse at the output & returns back to its stable state. The duration of the pulse depends on the values of R &C. It is also called as Mono shot or one shot MV.



Detailed Diagram of Monostable Multi-vibrator

Working:

Initially, let output be 0, then Q of FF is high & it holds the transistor Q1 on, thus clamping the external timing capacitor to ground. As the input trigger passes through $V_{cc}/3$, the FF is reset & hence Q=0.This makes Q_1 off & the short circuit across timing capacitor is released, & now output is high. Now the timing cycle begins, charging capacitor C towards V_{cc} through R with a time constant RC. After a time period T when the capacitor Voltage just exceeds $2/3V_{cc}$ (as compared in UC), the UC output becomes 1 & sets the FF output to 1.Therefore Q=1.Now transistor q1 turns on (saturates), thereby discharging the capacitor rapidly to ground potential. Output also returns to 0 state.



Waveforms of Monostable Multivibrator

Expression for Pulse Width:

The instantaneous Voltage across capacitor is given by,

$$V_c = V_f + (V_i - V_f)\, e^{-\tau / T_P}$$

Here V_f is the final voltage the capacitor can reach=V_{cc}

V_i is the initial voltage of the capacitor=0

Therefore, $V_c = V_{cc}(1-e^{-t/RC})$

But $V_c=2/3V_{cc}$ at $t=T_P$, the pulse width.

$$2/3V_{cc} = V_{cc}[1- e^{-T_P/RC}]$$

$$e^{-T_P/RC} = 1-2/3=1/3$$

$$^{-T_P/RC}=\ln(1/3)=-1.0986$$

$$T_P=1.1RC$$

Therefore Voltage across capacitor will reach $2/3V_{cc}$ in approximately 1.1RC which is also the pulse width.

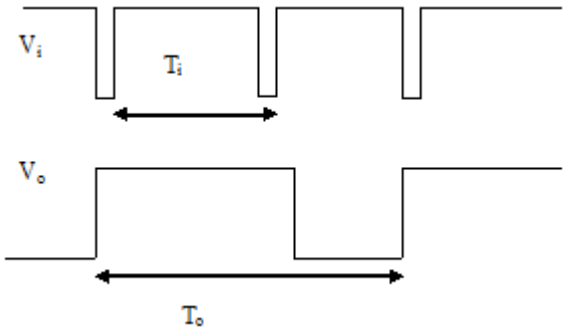
NOTE:

- Once triggered output remains in high state until the time T_P elapses which depend only on R & C. Any additional trigger pulse coming during this time will not alter the output states.
- But, if a negative going reset pulse is applied at pin 4 during the timing cycle, Q_2 turns on thereby over riding Q output of FF & Q_1 also turns on & external capacitor C is immediately discharged as shown in fig.
- Now even if Reset is released output will remain low till the next negative going trigger pulse comes along.

Applications of Monostable Multivibrator

Frequency Divider

Since the application of a trigger pulse causes output to go to high state, by adjusting time interval of input trigger to be less than the pulse width of the monostable multi-vibrator, it can be used as a frequency divider.

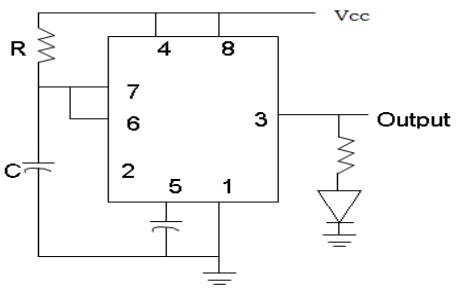


Waveform of Frequency Divider

In the above waveform $T_i>T_o$. Therefore $f_o=f_i/2$.

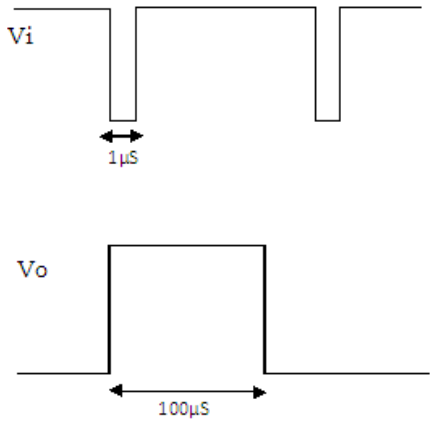
In general, if $T_i>$ (n-1) To, then $f_o= f_i/n$.

Pulse Stretcher



Pin Diagram of Pulse Stretcher

The monostable circuit shown above can also be called as a pulse stretcher if we consider its working where a narrow negative trigger pulse input is converted to a wide positive output pulse. This circuit is especially useful in LED displays where the display should be kept on for at least a sufficient duration of time so that it can be noticed by the human user (persistence of vision).The input & output pulses are as shown below:



Waveform of Pulse Stretcher

3. Draw the block diagram of an Astable multi-vibrator using 555 timer and derive an expression for its frequency of oscillation. (11) (NOV/2014)

(or)

Explain in detail about the Astable multi-vibrator. (APRIL/2012)

(or)

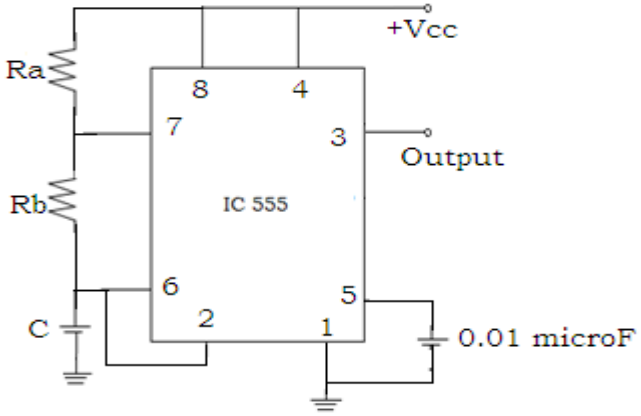
Explain the operation of Astable multi-vibrator with neat sketch. (NOV/2013)

(or)

Explain the operation of Astable multi-vibrator. (APRIL/2014)

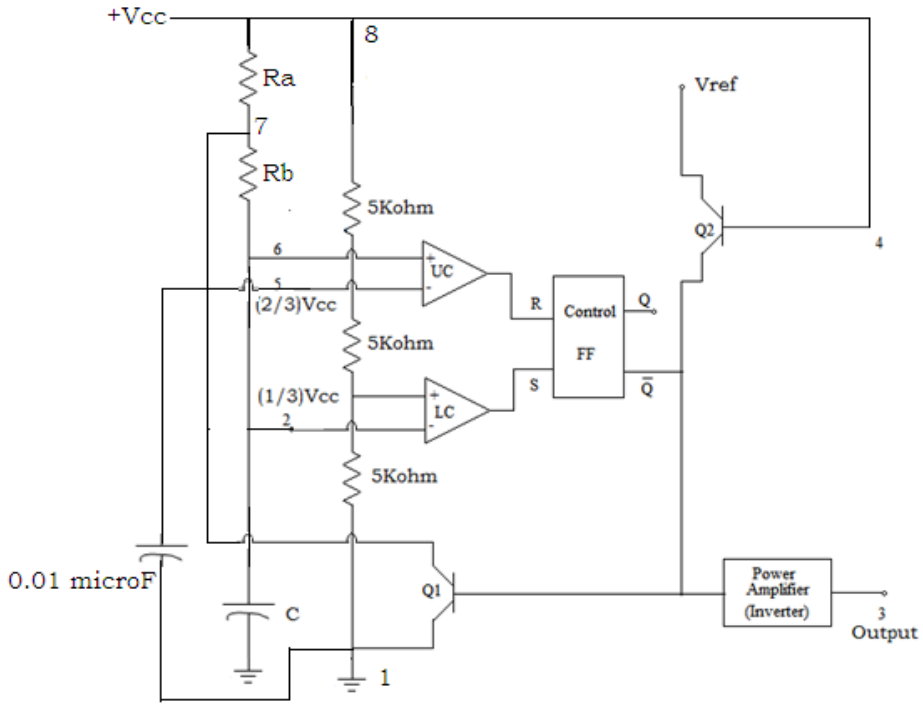
ASTABLE MULTIVIBRATOR USING IC 555

An Astable multi-vibrator is a regenerative comparator having no stable states but two quasi stable states. It is also called free-running multi-vibrator, because it does not require an external trigger pulse to change its output. The output continuously alternates between high & low states.



Pin Diagram of Astable Multi-vibrator

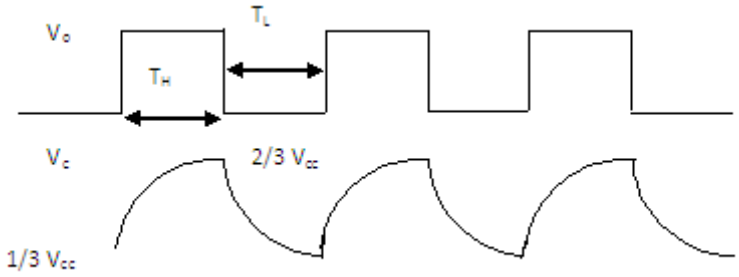
The time period for which the output remains in either of the states is determined by two timing resistors & a capacitor that are externally connected to the circuit.



Detailed Diagram of Astable Multi-vibrator

Working:

Comparing monostable operation, timing resistor is now split into two parts R_a & R_b. Pin 7, collector of discharging transistor Q1 is connected to the junction of R_a & R_b. Assume initially output is high. Output of FF, Q=0. The discharge transistor Q1 is off .Now the external timing capacitor charges towards V_{cc} with a time constant (R_a+ R_b) C. As the capacitor Voltage rises just above $2/3V_{cc}$, the output of UC becomes 1 & that of LC becomes 0 thereby setting the output of control FF to 1.Hence final output at pin 3 becomes 0. Now the discharge transistor Q1 is on & the capacitor discharges with a time constant (R_b)C.As the capacitor voltage just reaches below $1/3V_{cc}$ LC is triggered on & output of UC becomes 0 thereby making the output of FF 0 & final output high. This unclamps the timing capacitor C which now starts getting charged again repetitively.



Waveforms of Astable Multivbrator

<u>Expression for T</u>

The instantaneous voltage across the capacitor is given by,

$$V_c = V_f + (V_i - V_f)e^{-\tau/T}$$

Here, *V_f is the final voltage the capacitor can reach*

V_i is the initial voltage of the capacitor

Consider the charging time of capacitor as T_C

Now for charging,

$$V_f=V_{cc} \& \ V_i=1/3V_{cc}$$

Therefore,

$$V_c=V_{cc}+ (1/3V_{cc}-V_{cc})\ e^{-t/(Ra+Rb)C}$$

But

$V_c=2/3V_{cc}$ at $t=T_C$, the charging time.

Therefore,

$$2/3V_{cc}=V_{cc}+ (1/3V_{cc}-V_{cc})\ e^{-T_C/(Ra+Rb)C}$$

$$1/3V_{cc}=2/3V_{cc}e^{-T_C/(Ra+Rb)C}$$

$$e^{-T_C/(Ra+Rb)C}=1/2$$

$$T_C/(Ra+Rb)C=0.693$$

$$T_C=0.693(R_a+R_b)C$$

Now consider the discharging time of capacitor as T_D

For discharging,

$$V_f=0 \ \& \ V_i=2/3V_{cc}$$

Therefore,

$$V_c=0+ (2/3V_{cc}-0)\ e^{-t/RbC}$$

But

$V_c=1/3V_{cc}$ at $t=T_D$, the discharging time.

Therefore,

$$1/3V_{cc}=0+(2/3V_{cc}-0)e^{-T_D/RbC}$$

$$e^{-T_D/RbC}=1/2$$

$$T_D/R_bC=0.693$$

$$T_D=0.693R_bC$$

$$T=T_C+T_D$$

$$T=0.693(R_a+2R_b)\ C$$

$$f=1/T=1.45/(R_a+2R_b)C$$

Duty Cycle

The ratio of the time duration for which the output is high to the total time period T is called the duty cycle of the Astable multi-vibrator denoted by D.

$$D=T_C/T$$

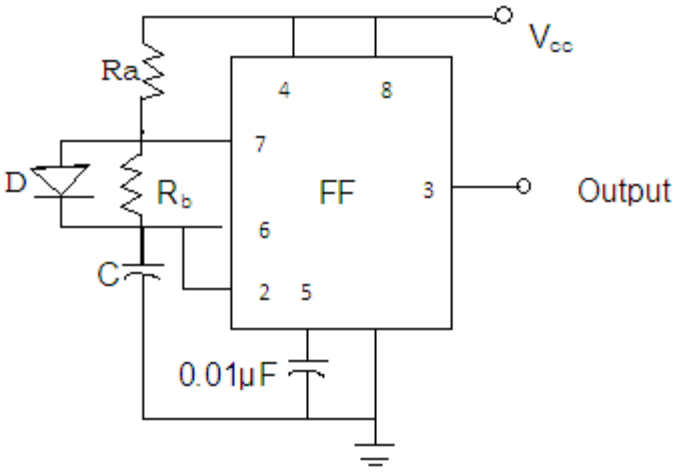
$$D = (R_a+R_b)/ (R_a+2R_b)$$

NOTE:

D can never be equal to or less than 0.5 for any combination of R_a & R_b ,& it is always greater than 0.5

To obtain a duty cycle of 50%, $R_a=0$ which results in an additional current through transistor Q1 hence damaging the transistor.

However there is an alternate solution to this problem. A switching diode is connected in parallel with R_b as shown in figure below.



Astable Multi-vibrator with Diode

In the above circuit, during the charging interval of the capacitor the diode is forward biased, it conducts & bypasses R_b. So the capacitor charges through R_a& diode D. But, as before it discharges through R_b. Then assuming ideal diode the charging & discharging intervals of the capacitor are:

$$T_C=0.693R_aC$$

$$T_C=0.693R_bC$$

$$T= 0.693(R_a+R_b)\ C$$

$$D= D=T_C/T = (R_a)/ (R_a+R_b)$$

If we set $R_a=R_b$, we get a duty cycle of 50% & a symmetrical square wave at the output.

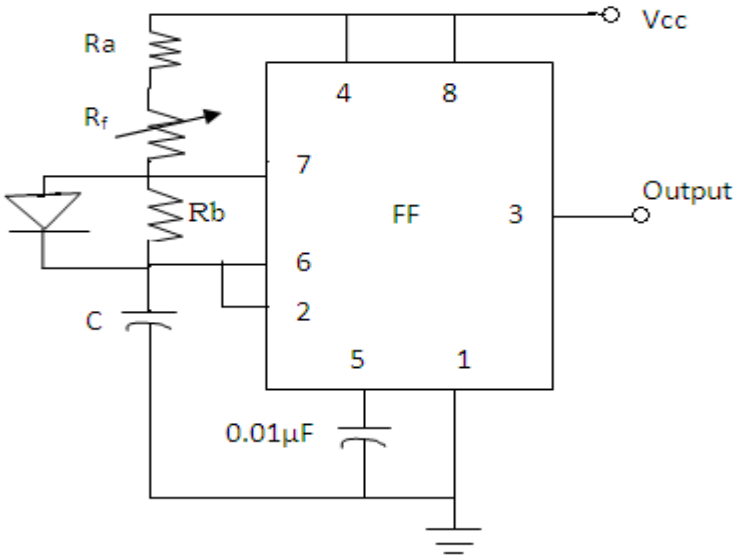
Design considerations for Monostable & Astable Multivibrators

- The timing capacitance should be larger than 500pF to keep stray capacitances negligible.
- The resistors should be greater than 1KΩ to limit the current & should not be larger than 3.3MΩ (the sum in case of Astable)
- Maximum frequency of oscillation is limited to 1MHz.

APPLICATIONS OF 555 ASTABLE MULTIVIBRATOR

Square Wave Generator

An astable multivibrator can be used as a square wave generator. To obtain a symmetrical square wave with 50% duty cycle the following circuit can be used. Here the capacitor charges through R_a & the forward biased diode D & discharges through R_b.In order to make the charging & discharging times equal, the resistance R_a is constructed with a fixed resistance in series with a potentiometer as shown in figure, so that the potentiometer can be adjusted to get $R_a+R_f =R_b$ in order to obtain an exact symmetrical square wave output where R_f is the forward resistance of the diode



Square Wave Generator

Free Running ramp Generator

The 555 Astable multi-vibrators can be used to generate a free running ramp by replacing the timing resistors R_a & R_b with a current mirror as shown below. Here the current mirror acts as a constant current source & charges the capacitor C linearly towards V_{cc}. When the capacitor voltage rises above $2/3V_{cc}$ the UC sets the FF output to 1 which in turn turns on the discharge transistor Q1 on. Thus, the capacitor discharges rapidly through transistor Q1.When the capacitor voltage drops below 1/3vcc LC output resets the FF output to 0 which causes the discharge transistor to turn off & as a result the capacitor C begins to charge again.

The charging & discharging of the capacitor repeats continually resulting in the waveform shown in fig. Also $T_c>>T_D$ because the capacitor discharges through the on transistor whose resistance is very small. Hence $T=T_c$. During the charging time Tc, the capacitor voltage changes by $1/3V_{cc}$ due to the flow of the constant current I_c. The charge acquired by the capacitor C as a result of the constant current I_c flowing for a time t_c is given by,

$$Q=I_c t_c$$

The charge acquired by a capacitor of capacitance C is also given by

$$Q=CV$$

Where, V is the change in voltage across the capacitor.

In this case, since $V=1/3V_{cc}$ we have

$$Q=1/3V_{cc}$$

Hence, from equations (13) & (14), we get

$$t_c I_c=1/3V_{cc}C$$

The period of the free running ramp is $T=t_c$& therefore,

$$T=t_c=V_{cc}C/3I_c$$

Where the constant current I_c is given by,

$$I_c=V_{cc}-V_{BE}/R$$

The free running frequency of the ramp generator is thus

$$f=1/T=3I_c/V_{cc}\,C$$

4. Design a monostable multi-vibrator for a pulse width of 1ms.

T_P=1ms=1.1RC

Let C=0.1µF

Then R=1ms/ $(1.1*0.1*10^{-6})$ = 9.1KΩ

5. A 555 monostable multi-vibrator is used to divide a 1 KHz input signal by 3.If R=20K, calculate the required value of C.

The period of the trigger input signal is

T_t=1/1 KHz = 1ms.

For a divide by 3 circuit, T_P should be greater than $2T_t$ but less than $3T_t$.Let us take $T_P=2.2T_t$

Therefore T_P=2.2*1ms=2.2ms

Thus $C=T_P/1.1R=2.2*10^{-3}/1.1*20*10^{3}$=0.1µF

6. Design a 555 mono-stable circuit that stretches the width of a narrow pulse from 1µs to 100µs.

The width TP of the mono-stable output should be 100µs.Therefore,

$RC=T_P/1.1=100*10^{-6}/1.1=90.9*10^{-6}$

Let C=0.1µF, we have

$R=90.9*10^{-6}/C = 90.9*10^{-6}/0.1*10^{-6}$ =909Ω.

7. Design a 555 timer astable multivibrator for an output frequency of 1 KHz & duty cycle of 60%.

T = 1/f = 1/1 KHz = 1ms

T_C=TD=0.6*1ms=0.6ms

$T_D=T- T_C$ = (1-0.6)ms=0.4ms

$R_b=T_D/0.693C$

Let C=0.1µF

Therefore $R_b=0.4*10^{-3}/0.693*0.1*10^{-6}$ = 5.77K Ω

$R_a=T_C/0.693C - R_b$

3.06K Ω.

8. What is meant by counters and explain any one type of counters

COUNTERS

A counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. In practice, there are two types of counters:

- Up counters, which increase (increment) in value
- Down counters, which decrease (decrement) in value

Counters can be implemented easily using register-type circuits such as the flip-flop. The types of counters are

- Asynchronous (ripple) counter – changing state bits are used as clocks to subsequent state flip-flops
- Synchronous counter – all state bits change under control of a single clock
- Decade counter – counts through ten states per stage
- Up–down counter – counts both up and down, under command of a control input
- Ring counter – formed by a shift register with feedback connection in a ring
- Johnson counter – a twisted ring counter
- Cascaded counter

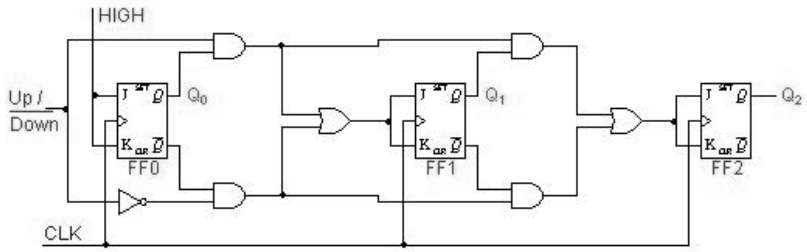
9. Explain the operation of UP/DOWN counter (APRIL/2012)

(or)

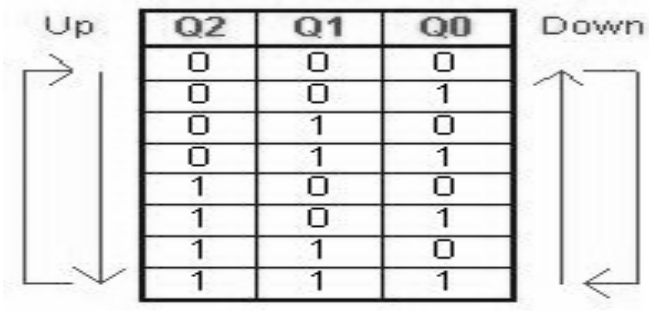
Draw and explain the operation and truth table of UP-DOWN counter. (APRIL/2013)

Up Down counters

A circuit of a 3-bit synchronous up-down counter and a table of its sequence are shown below. It is used to control the direction of the counter through a certain sequence.



Synchronous counter



Q2	Q1	Q0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

Bit Sequence

- For both the UP and DOWN sequences, Q0 toggles on each clock pulse.
- For the UP sequence, Q1 changes state on the next clock pulse when Q0=1.
- For the DOWN sequence, Q1 changes state on the next clock pulse when Q0=0.
- For the UP sequence, Q2 changes state on the next clock pulse when Q0=Q1=1.
- For the DOWN sequence, Q2 changes state on the next clock pulse when Q0=Q1=0.

These characteristics are implemented with the AND, OR & NOT logic connected as shown in the logic diagram above.

10. Draw and explain the operation of shift registers. (APRIL/2014) (NOV/2013)

Shift registers

In digital circuits, a shift register is a cascade of flip flops, sharing the same clock, which has the output of anyone but the last flip-flop connected to the "data" input of the next one in the chain, resulting in a circuit that shifts by one position the one-dimensional "bit array" stored in it, shifting in the data present at its input and shifting out the last bit in the array, when enabled to do so by a transition of the clock input. A shift register may be multidimensional; such that its "data in" input and stage outputs are themselves bit arrays: this is implemented simply by running several shift registers of the same bit-length in parallel. Shift registers can have both parallel and serial inputs and outputs. These are often configured as serial-in, parallel-out (SIPO) or as parallel-in, serial-out (PISO). There are also types that have both serial and parallel input and types with serial and parallel output. There are also bi-directional shift registers which allow shifting in both directions: L→R or R→L. The serial input and last output of a shift register can also be connected together to create a circular shift register.

11. ***Explain the working of serial in – serial out shift register with logic diagram. (NOV/2012)***

Serial-In, Serial-Out (SISO)

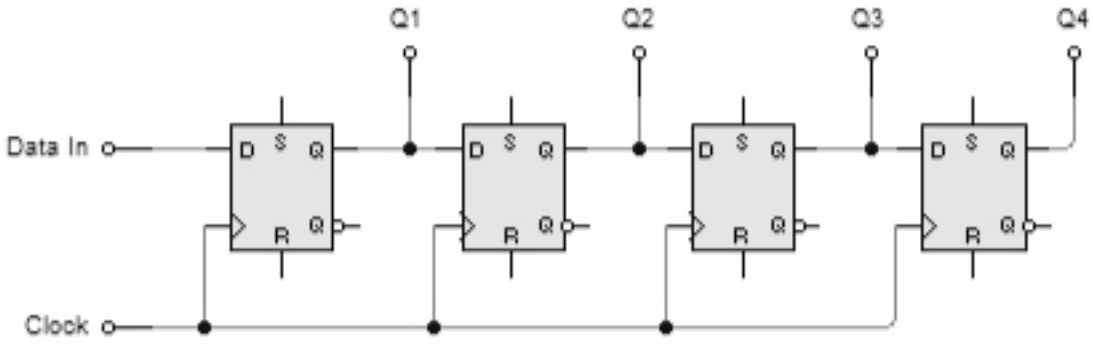
Serial-IN Serial-OUT register is simplest kind of shift registers. The data string is presented at 'Data In', and is shifted right one stage each time 'Data Advance' is brought high. At each advance, the bit on the far left (i.e. 'Data In') is shifted into the first flip-flop's output. The bit on the far right (i.e. 'Data Out') is shifted out and lost. The data are stored after each flip-flop on the 'Q' output, so there are four storage 'slots' available in this arrangement; hence it is a 4-Bit Register. To give an idea of the shifting pattern, imagine that the register holds 0000 (so all storage slots are empty). As 'Data In' presents 1,0,1,1,0,0,0,0 (in that order, with a pulse at 'Data Advance' each time. This is called clocking or strobing) to the register, this is the result. The left hand column corresponds to the left-most flip-flop's output pin, and so on. So the serial output of the entire register is 10110000.

0	0	0	0
1	0	0	0
0	1	0	0
1	0	1	0
1	1	0	1
0	1	1	0
0	0	1	1
0	0	0	1
0	0	0	0

4 Bit Sequence of Serial In Serial Out Shift Register

Serial-In, Parallel-Out (SIPO):

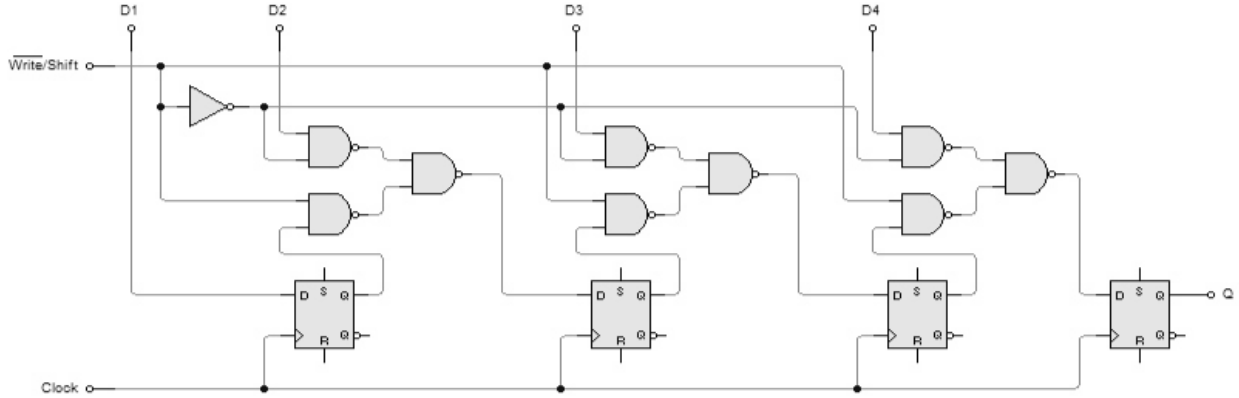
This configuration allows conversion from serial to parallel format. Data is input serially. Once the data has been input, it may be either read off at each output simultaneously, or it can be shifted out and replaced.



4-Bit SIPO Shift Register

Parallel-In, Serial-Out (PISO)

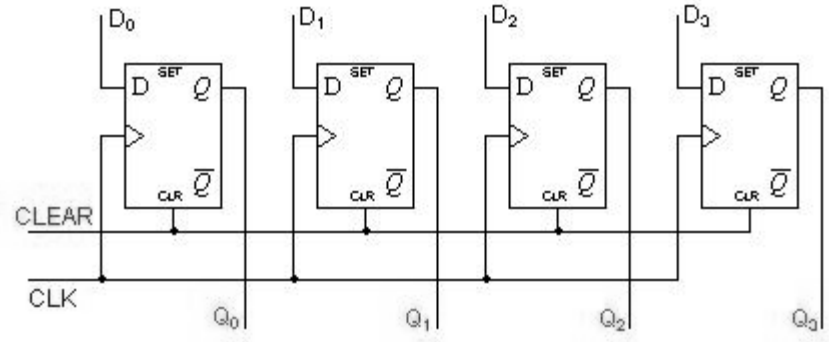
This configuration has the data input on lines D1 through D4 in parallel format. To write the data to the register, the Write/Shift control line must be held LOW. To shift the data, the Write/Shift control line is brought HIGH and the registers are clocked. The arrangement now acts as a PISO shift register, with D1 as the Data Input. However, as long as the number of clock cycles is not more than the length of the data-string, the Data Output, Q, will be the parallel data read off in order.



4 Bit Parallel In Serial Out Shift Register

Parallel In Parallel Out Register

For parallel in - parallel out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits. The following circuit is a four-bit parallel in - parallel out shift register constructed by D flip-flops.



4Bit Parallel Bit Parallel Out Shift Register

The D's are the parallel inputs and the Q's are the parallel outputs. Once the register is clocked, all the data at the D inputs appear at the corresponding Q outputs simultaneously.

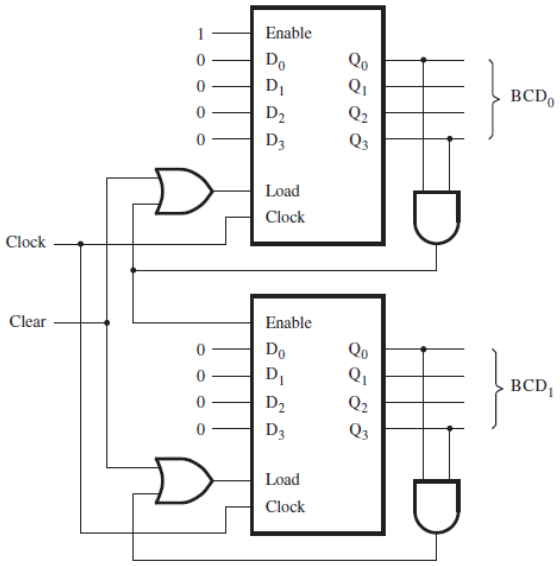
Applications:

- One of the most common uses of a shift register is to convert between serial and parallel interfaces. This is useful as many circuits work on groups of bits in parallel, but serial interfaces are simpler to construct. Shift registers can be used as simple delay circuits. Several bi-directional shift registers could also be connected in parallel for a hardware implementation of a stack.
- Shift registers can be used also as pulse extenders. Compared to monostable multi-vibrators the timing has no dependency on component values, however requires external clock and the timing accuracy is limited by a granularity of this clock.
- shift registers were used to handle data processing: two numbers to be added were stored in two shift registers and clocked out into an arithmetic and logic unit (ALU) with the result being fed back to the input of one of the shift registers (the Accumulator) which was one bit longer since binary addition can only result in an answer that is the same size or one bit longer.
- Many computer languages include instructions to 'shift right' and 'shift left' the data in a register, effectively dividing by two or multiplying by two for each place shifted.

12. Explain in detail about BCD counter

BCD Counter

Binary-coded-decimal (BCD) counters consists of two modulo-10 counters, one for each BCD digit, implemented using the parallel load four-bit counter. It is necessary to reset the four flip-flops after the count of 9 has been obtained. Thus the Load input to each stage is equal to 1 when Q3 = Q0 = 1, which causes 0s to be loaded into the flip-flops at the next positive edge of the clock signal. Whenever the count in stage 0, *BCD* 0, reaches 9 it is necessary to enable the second stage so that it will be incremented when the next clock pulse arrives.



BCD Counter

This is accomplished by keeping the Enable signal for *BCD*1 low at all times except when *BCD*0 = 9. It has to be possible to clear the contents of the counter by activating some control signal. Two OR gates are included in the circuit for this purpose. The control input clear can be used to load 0s into the counter. Clear is active when high. In any digital system there is usually one or more clock signals used to drive all synchronous circuitry. Counters can be used to count the number of pulses in any signal that may be used in place of the clock signal.

13. Explain in detail about Multiplexor and Demultiplexor

Multiplexors

"The multiplexor (mux), provides the function of a rotary switch, selecting one of several inputs to connect to a single output. The multiplexor is often referred to as a selector."

A mux acts like a rotary switch connecting one of several inputs to a single output. The selection of which input to connect to the output is determined by additional inputs called select or control lines. The input selected is determined by the binary equivalent of the value placed on the select lines. For example, consider a mux that selects one of four inputs to connect to the output. This is referred to as a 4-to-l mux. To select one of four inputs, there must be four unique combination of the select lines. This requires two select lines providing the four unique combinations 00, 01, 10, and 11. A select-line combination of 00 would select input 0, select-line combination 01 would select input I, and so on.

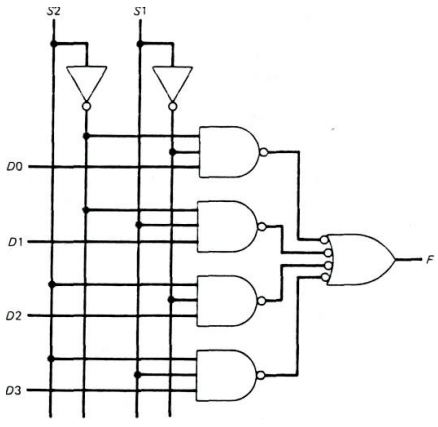
S1	S2	F
0	0	D0
0	1	D1
1	0	D2
1	1	D3

4-to-1 Mux Truth Table

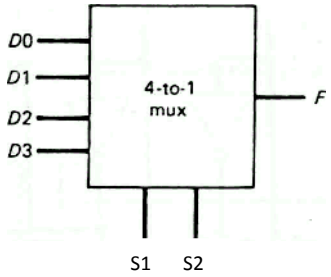
The function of the multiplexor is illustrated in the truth table shown in the above table. This truth table shows the output F as a function of the select-line inputs. Instead of listing all possible states of the data inputs, this simplified form of a truth table show the output as the data from input line 0 (DO), or input line 1 (D 1), and so on. As can be seen from the above table, we want to pass DO when 5'2 and 5'! are both 0. Likewise, we want to pass D 1 when 52 is 0 and S1 is 1, and so on for the remaining input combinations. This is implemented by the following expression:

$$F = \overline{S2}\,.\,\overline{S1}.DO + \overline{S2}.S1.DI + S2.\overline{S1}D2 + S2.S1.D3$$

The figure shown below is a NAND-gate implementation of a 4-to-l multiplexor. To better illustrate the function of the multiplexor as a complete "unit," all variable complement! have been generated internally. Since the multiplexor function is so useful, many TTL chips exist that perform the equivalent operation of the circuit shown in below figure. For example, the 7415; contains two 4-to-l multiplexors, the 74151 contains one 8-to-l multiplexor, and the(74157 contains four 2-to-l multiplexors. A multiplexor is typically shown in a circuit as a single functional unit, not as the gates comprising the circuit. A typical representation of a 4-to-l multiplexor is shown in below figure.



4-to-l Mux Implementation



4-to-l Mux Representation

The Demultiplexor

"The demultiplexor (demux), provides the inverse function, connecting a single input to one of several outputs. The demultiplexor is often referred to as a decoder."

The demultiplexer connects one input to one of several outputs. The output is selected via select lines as it is with the mux. The most common use of a demultiplexer is as a decoder. In fact, demuxes are typically referred to as decoders. A decoder sets the output line selected by the select lines to 0. This function is easily implemented with the demux by tying the data input line to 0.

To illustrate the behavior of a demux, consider the operation of a demux that connects one input to one of four outputs. This is referred to as a l-to-4 demultiplexer. Used as a decoder, it is referred to as a 2-to-4 decoder since two select lines select one of four outputs. The operation of this demux is illustrated in the below table. This truth table shows the four outputs of the demux as a function of the data in D 1 and select lines.

Notice that the default state of an output is 1. Therefore, any outputs not selected will be 1. Thus, as table shown below illustrates, when the data in D1 input is 1, all outputs will be 1 regardless of the select-line combination.

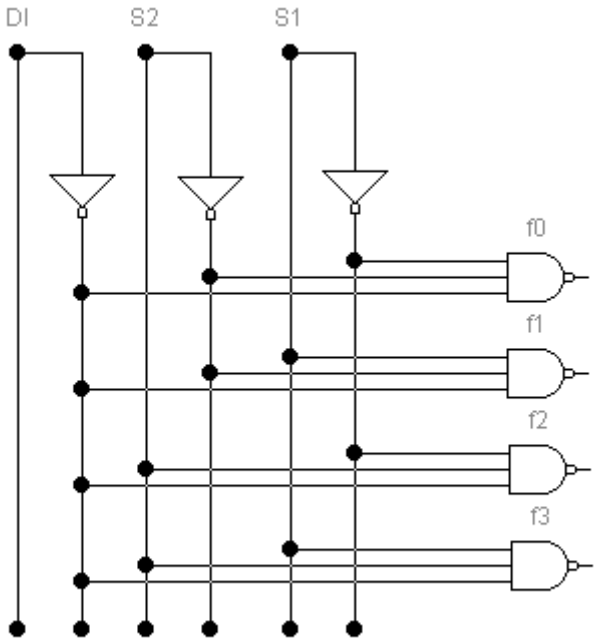
A decoder sets the output selected by the select-line inputs to 0. As can be seen in the below table, this is accomplished by tying the data input to 0. Thus the data input can be thought of as an active-low enable for the decoder. If this enable is not low, the decoder will not function (all outputs will always be 1). Often decoders will have more than one enable line, requiring all enable lines to be properly enabled before the decoder functions.

The functions illustrated in the below table can be expressed algebraically as:

$$FO = \overline{\overline{D1}}\ \overline{\overline{S2}}\ \overline{\overline{S1}}$$
$$F1 = \overline{\overline{D1}}\ \overline{\overline{S2}}\ \overline{S1}$$
$$F2 = \overline{\overline{D1}}\ \overline{S2}\ \overline{\overline{S1}}$$
$$F3 = \overline{\overline{D1}}\ \overline{S2}\ \overline{S1}$$

D1	S2	S1	F0	F1	F2	F3
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0
1	X	X	1	1	1	1

l-to-4 Demux Truth Table



l-to-4 Demux Implementation

The figure shown above is a NAND-gate implementation of the l-to-4 demux (2-to-4 decoder). As with multiplexors, the demultiplexor circuit is available in several variations on standard TTL chips. For example, the 74138 contains one l-to-8 demux (3-to-8 decoder), and the 74139 contains two l-to-4 demuxes (2-to-4 decoders).

As with the multiplexor, a demux is typically shown in a circuit as a separate functional unit, not as the gates comprising the demux. Shown in the above figure are typical demux and decoder representations of the circuit in figure. Note the presence of active-low indicators at the enable input and each of the outputs on the decoder representation. This indicates the decoder is enabled with a low input, and an output is set to low when selected.

Applications of MUX and DEMUX

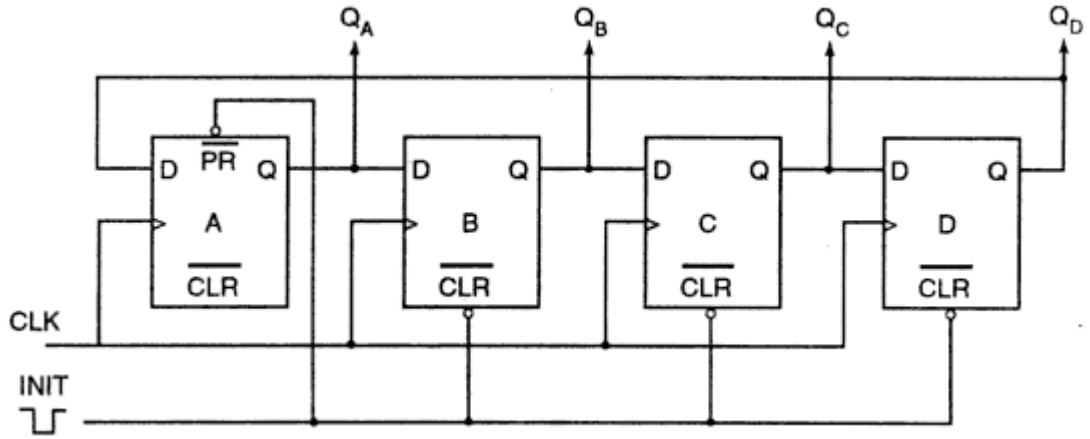
Used in tandem, a mux-demux combination can be used for serial communication to reduce the number of wires required to pass data. The pair can be used in a similar manner to run multidigital displays such as those found in calculators. Muxes are often used in digital circuits to control signal and data routing. For example, a multiplexor can be used to select the input to a particular register from one of several sources. Decoders are often used in computers to provide address decoding. Based on certain address lines, the decoder can provide enable signals to the proper memory chips. In addition, both muxes and demuxes can be used to evaluate simple boolean expressions using less hardware than if individual logic gates were used.

14. Explain about ring counter with neat diagram.

Ring counter

In a ring counter, the true output (Q) of the last flip-flop in a shift register is connected back to the serial input of the first flip-flop, and also only one flip-flop is set at any particular time while all others are cleared. The flip-flops are connected in such a way the information shifts either from left to right and back around from Q_D to Q_A or from right to left and back around from Q_A to Q_D. Single a single 1 in the register is made to circulate around the register as long as clock pulses are applied, it is called ring counter.

A 4- bit ring counter using D flip-flops is shown in the below figure. This circuit consists of four D flip-flops and their outputs are Q_A, Q_B, Q_C and Q_D respectively. The PRE-SET input of first flip-flops and CLEAR inputs of the other three flip-flops are connected together and brought out as INIT input. Now, on applying a LOW pulse at this INIT input, the first flip-flop is SET to 1 and the other three flip-flops are cleared to 0, i.e. $Q_AQ_BQ_CQ_D = 1000$. Now, from this circuit it is clear that $D_A= 0$, $D_B = 0$, $D_C = 0$ and $D_D = 0$. Therefore, when a clock pulse is applied, the second flip-flop is set to 1 while the other three flip-flops are reset to 0, i.e. the output of the ring counter $Q_AQ_BQ_CQ_D = 0100$. As a result, on the occurrence of the first clock pulse, the 1 in the first flip-flop shifted to the second flip-flop. Similarly, when the second clock pulse is applied, the 1 in the second flip-flop is shifted to the third flip-flop and the ring counter output $Q_AQ_BQ_CQ_D = 0010$; on the occurrence of the fourth clock pulse, the output will be $Q_AQ_BQ_CQ_D = 0001$; on the fifth clock pulse, $Q_AQ_BQ_CQ_D = 1000$, i.e. the initial state. Thus, 1 is shifted or circulated around the register as long as clock pulses are applied. The truth table which describes the operation of the above 4-bit ring counter is shown in the table.



A 4 –bit counter using D- flip-flop

INIT	CLK	Q_A	Q_B	Q_C	Q_D
L	X	1	0	0	0
H	↑	0	1	0	0
H	↑	0	0	1	0
H	↑	0	0	0	1
H	↑	1	0	0	0

Truth table for 4-bit ring counter

As shown in the above truth table, the ring counter has only 4 valid states, i.e. 1000, 0100, 0010 and 0001. The ring counter can hang or enter into anyone of the invalid state due to noise or any other condition without returning to the main counting sequence. Hence, it is a must to design ring counters which are self- correcting and capable of recovering from invalid states to valid states.

Reference:

1. *I. Albert Malvino and David Bates, "Electronic Principles", 7th Edition, Tata Mc-Graw Hill, New Delhi, 2006.*
2. *Ramakant A Gayakward, Operational Amplifiers and Linear Integrated circuits, 4th Edition, PHI Learning, Delhi, 2009.*